



INVESTOR MEETING 2013

November 21, Santa Clara, CA



Advancing Moore's Law: Benefits Across the Portfolio

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Agenda

Fundamentals of Moore's Law
Cost, Capability, Performance/Watt

Reducing Cost in a Capital
Intensive Environment

Applying the Benefits Across the
Product Portfolio



Brief Update on 14nm Status

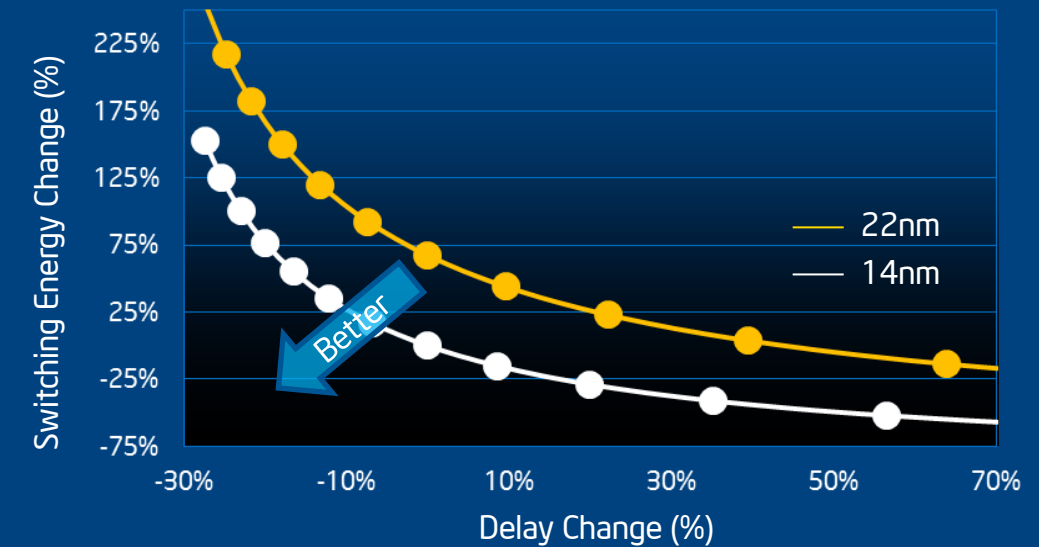
Yield

at the same point in development



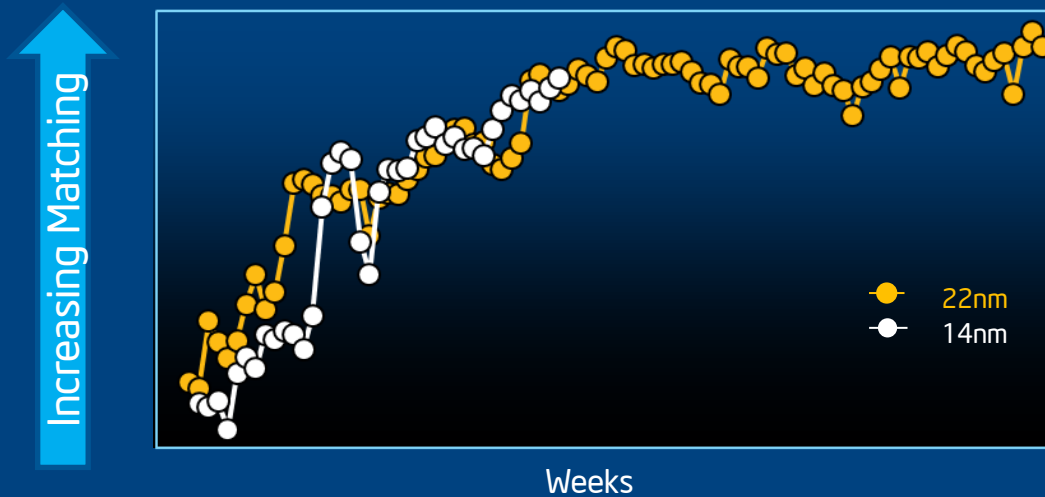
Performance Improvement

Switching Energy vs. Gate Delay



Key Parameter Matching

% of key process parameters meeting 3-sigma targets at the same point in development



14 nm key process parameter matching on track with 22 nm trend

Reliability Scorecard

at the same point in development

Module

Transistor
Interconnect
Thermo-Mechanical/Moisture
Test Vehicle Yield
ESD/LU
Alpha Particle/Soft Error

22nm
(2 year offset) 14nm

Transistor	Low risk	Low risk
Interconnect	Low risk	Low risk
Thermo-Mechanical/Moisture	Medium risk	Low risk
Test Vehicle Yield	Medium risk	Medium risk
ESD/LU	Low risk	Low risk
Alpha Particle/Soft Error	Medium risk	Low risk

Low risk
Meeting all cert goals

Medium risk
Close to meeting goals

High risk
Not yet meeting all goals, needs additional work

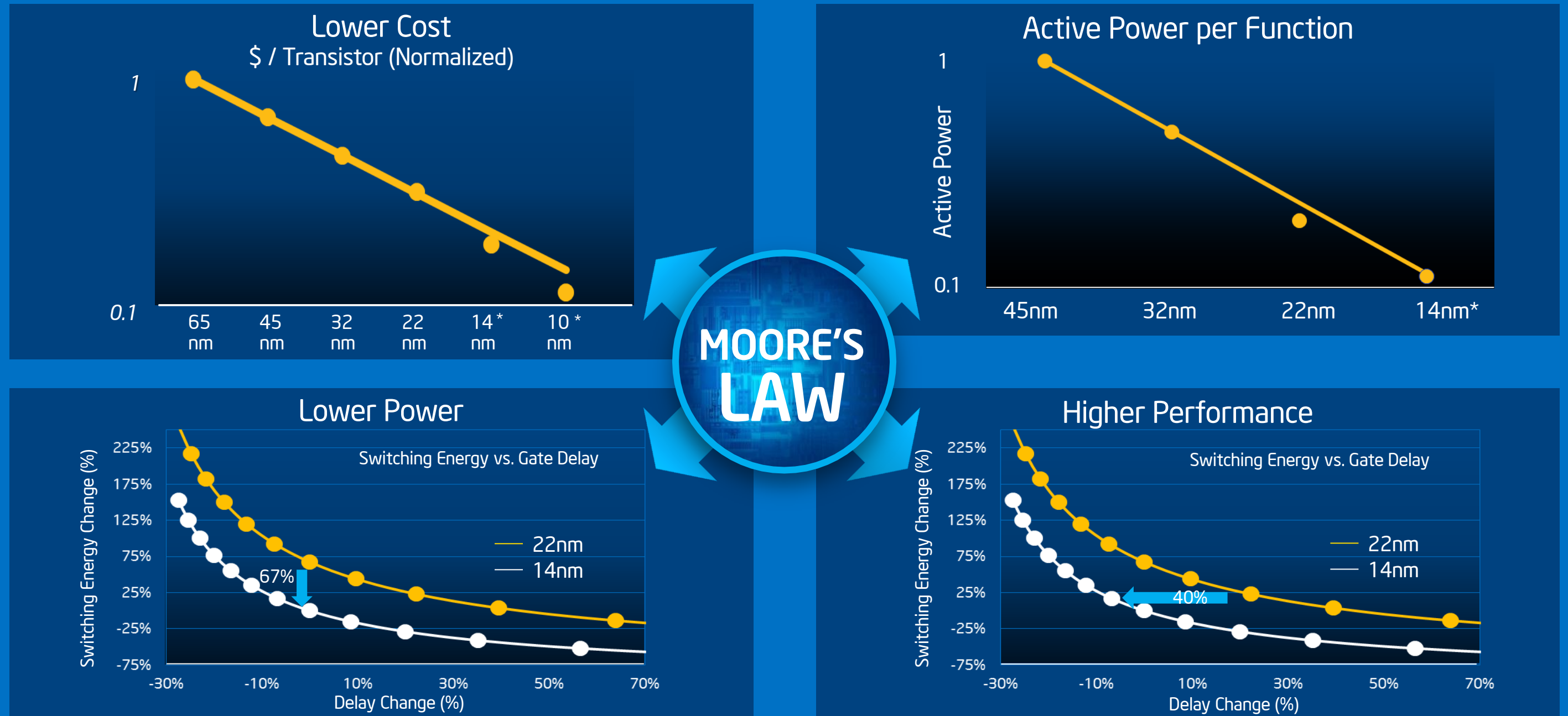
Generally healthy reliability at this stage, on track for Q1 '14 certification *

Fundamentals of Moore's Law

Reducing Cost in a Capital Intensive Environment

Applying the Benefits Across the Product Portfolio

Getting Benefits of Moore's Law Across all Value Vectors

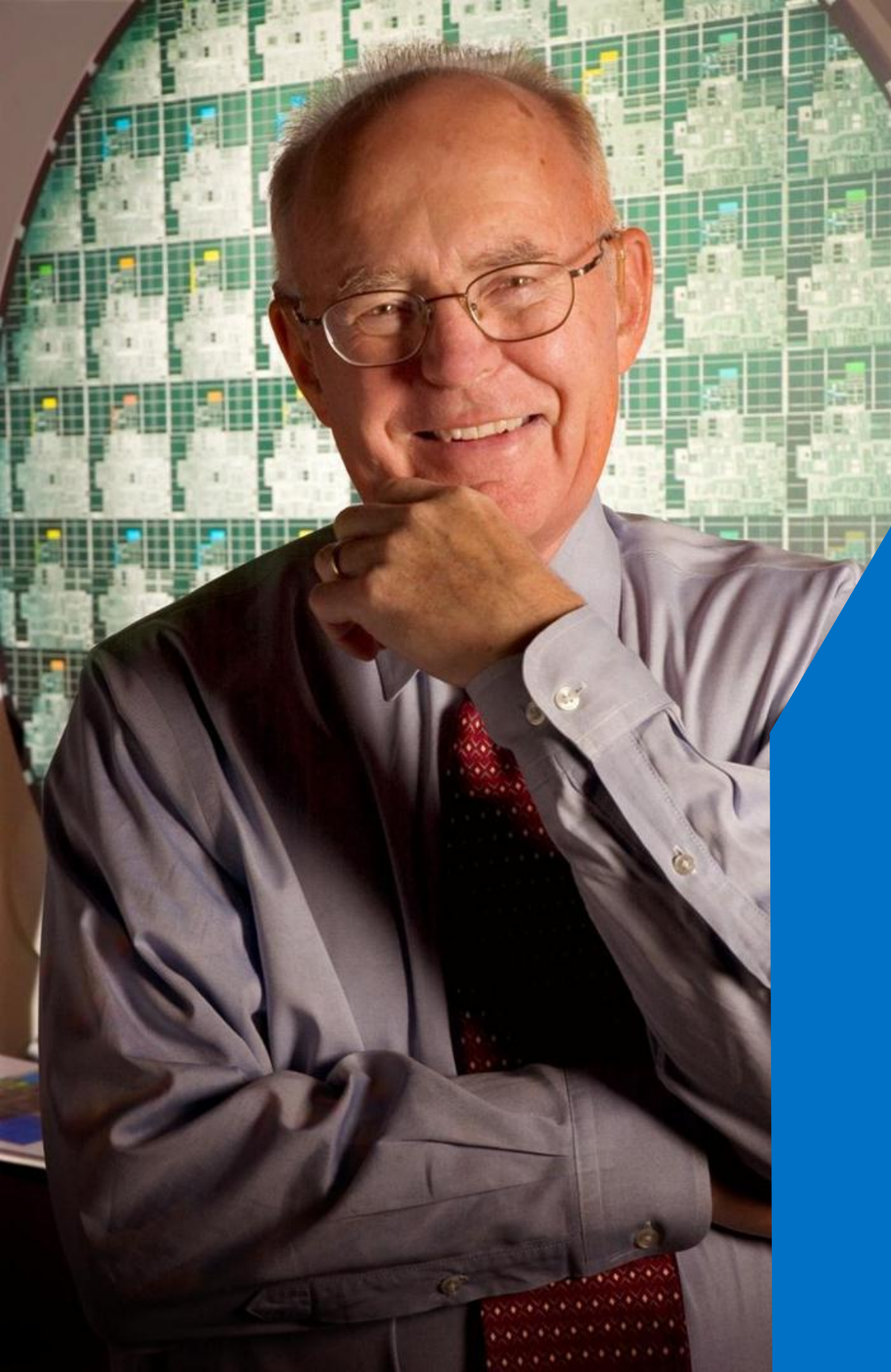


Source: Intel
* Forecast

Fundamentals of Moore's Law

Reducing Cost in a Capital Intensive Environment

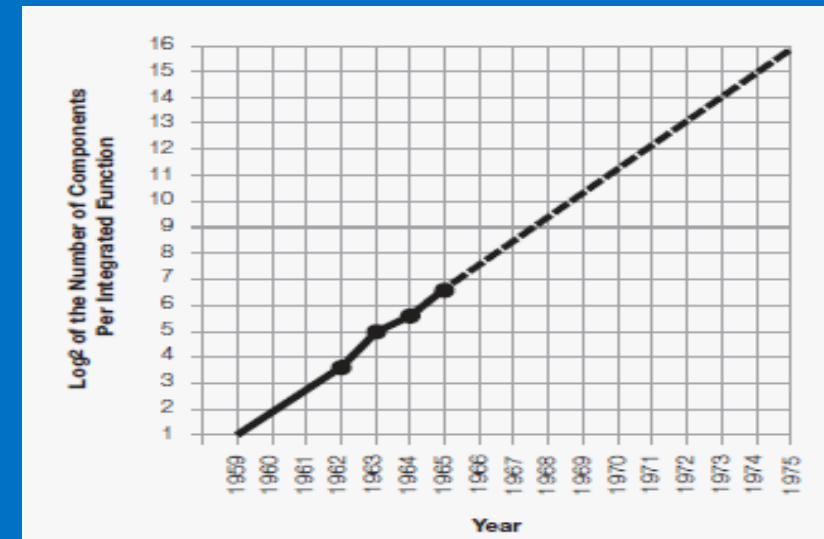
Applying the Benefits Across the Product Portfolio



Moore's Law – It's All About Economics

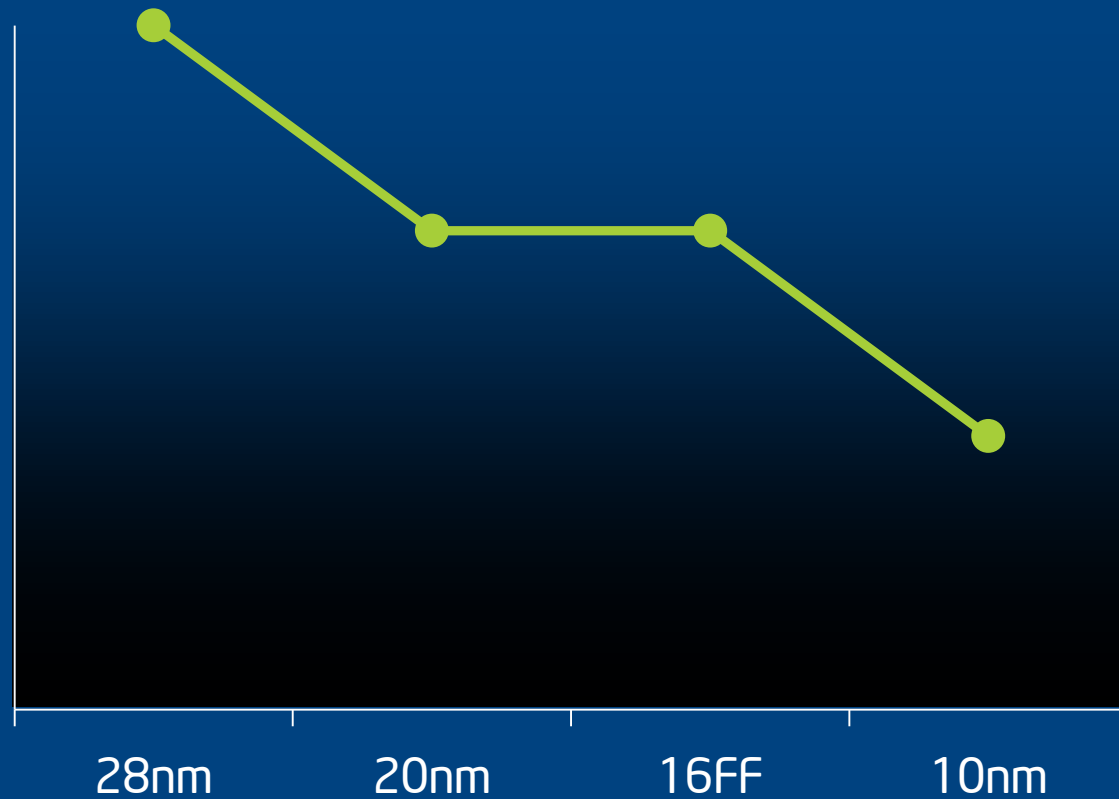
“Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate.”

Electronics, Volume 38, Number 8, April 19, 1965

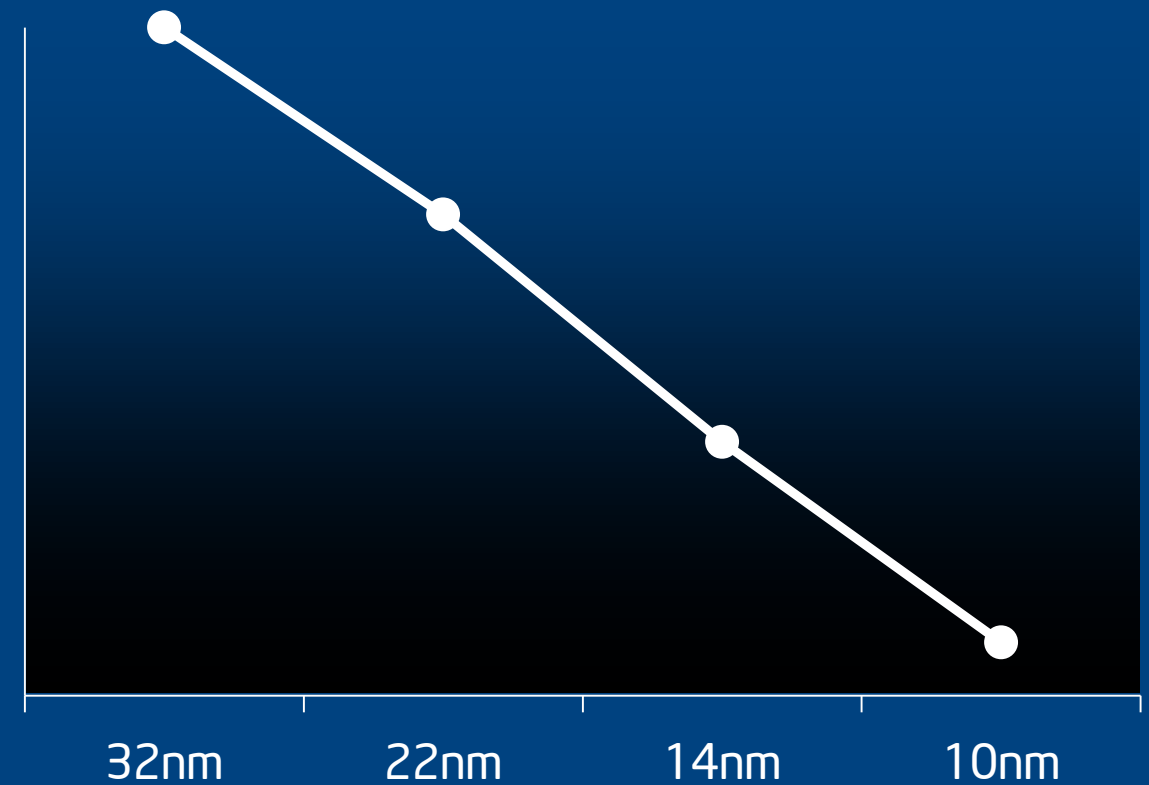


Competitors Projecting No Chip Area Scaling

Competitor Area Scaling
(normalized to 28nm)



Intel Area Scaling
(normalized to 32nm)



Competitor area scaling source: ARM Tech Con 2012, TSMC Keynote. Oct. 30, 2012 * Forecast

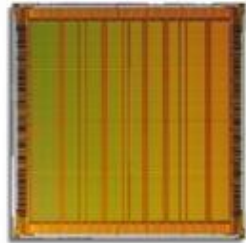
Intel is Continuing to Scale While Others are Pausing to do FinFETs

Our Customers See the Same Indicators

Altera vs. Xilinx Roadmap Comparison

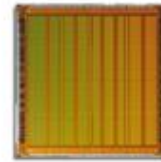
Altera

TSMC "20 SoC"
20nm Planar



Significant shrink
& performance gain

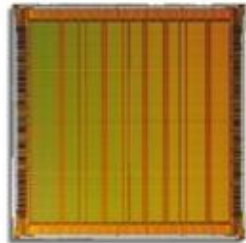
Intel "14nm TriGate"
14nm FinFET



- ✓ Higher Performance
- ✓ Lower Power
- ✓ Lower Cost

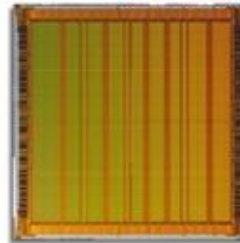
Xilinx

"20 SoC"
20nm Planar



Higher cost

"16FF"
20nm FinFET



Altera to capture high end FPGA market

Note: Altera relative die size estimates for equivalent capacity devices

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1

Stratix 10 Delivering the Unimaginable



1 GHz

2X

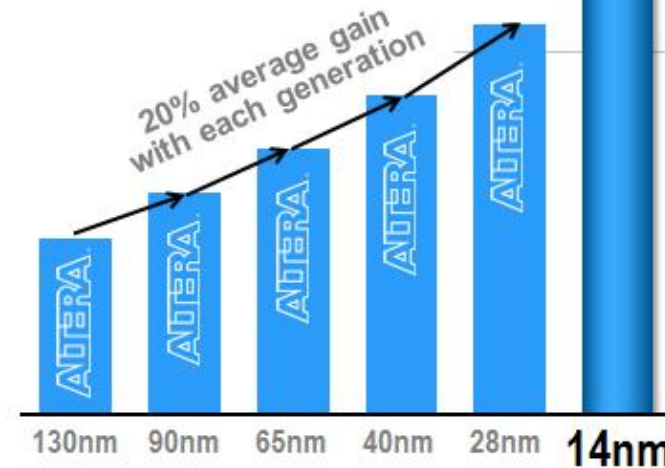
500 MHz

**Highest Performance
FPGAs and SoCs**

- Intel 14 nm  Tri-Gate process



- Enhanced high-performance architecture

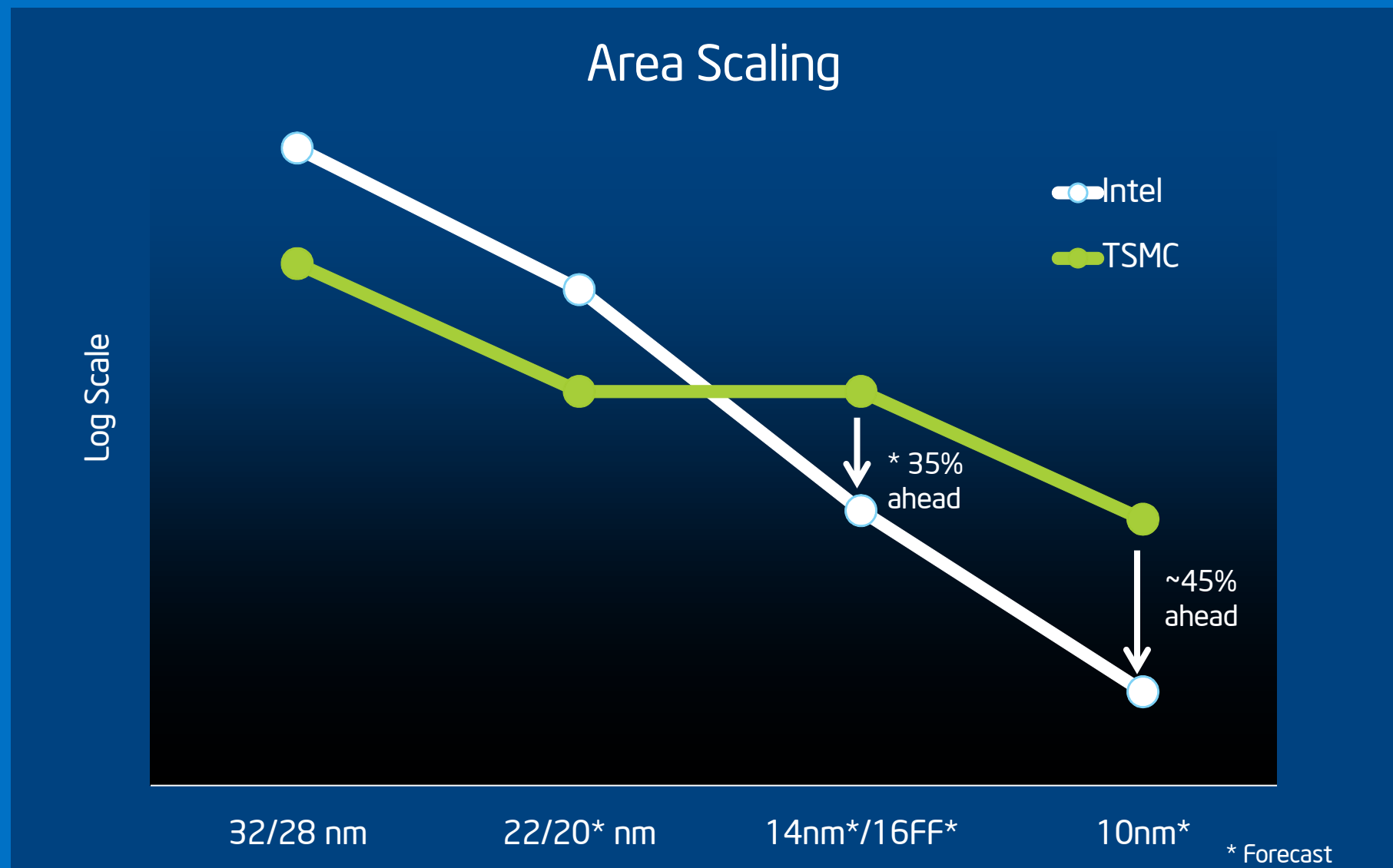


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2

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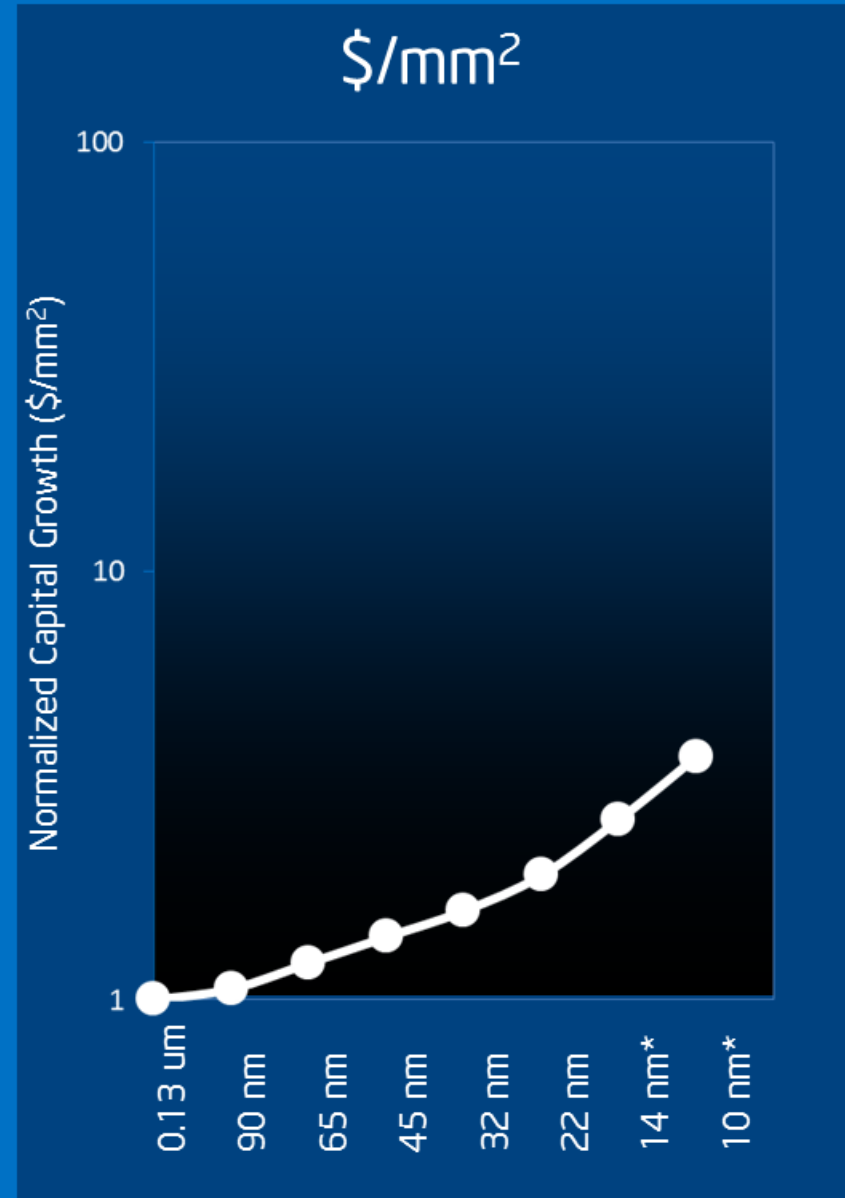
Intel Is Committed to Press Ahead on Density



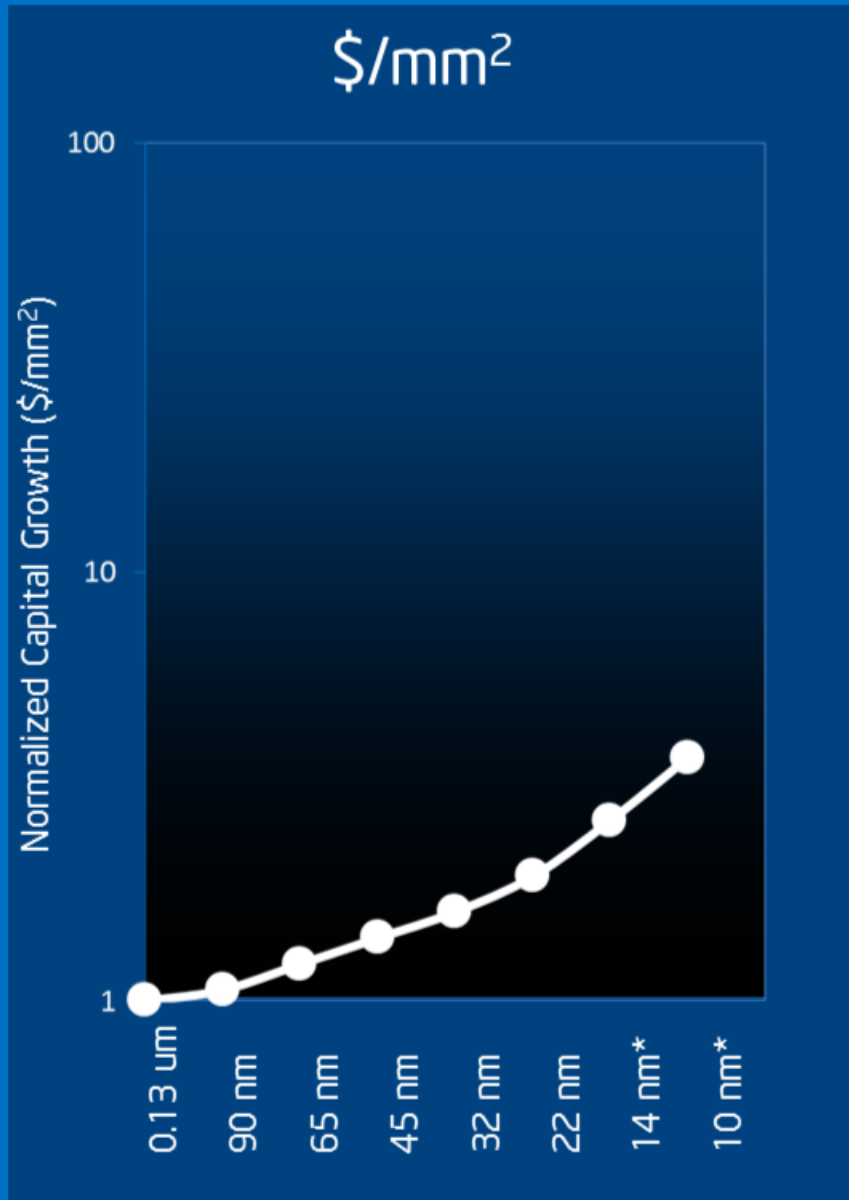
Sources: TSMC keynote, ARM Tech Con 2012, Oct. 30, 2012. Intel data Alignment based on internal assessment

Enables a "Transistor Like" Lead in Density

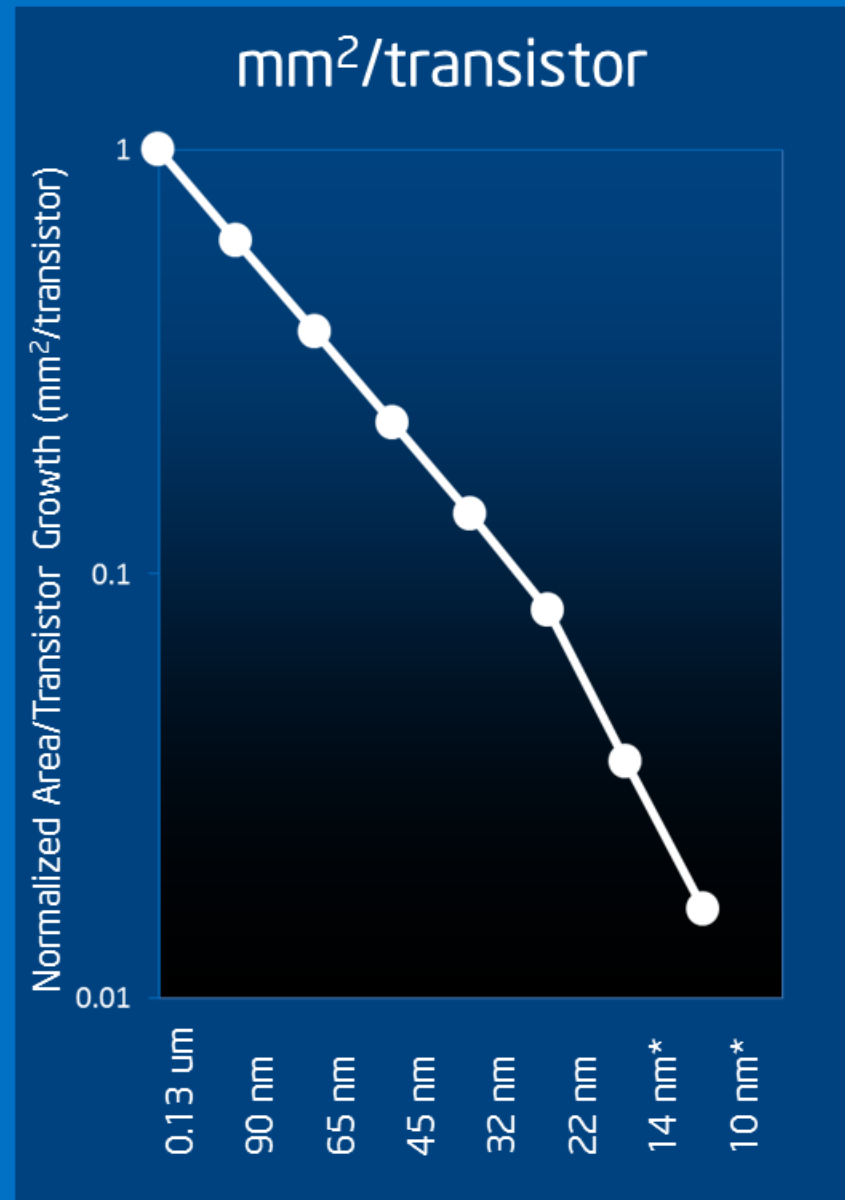
Density Improvements Offset Wafer Cost Trends



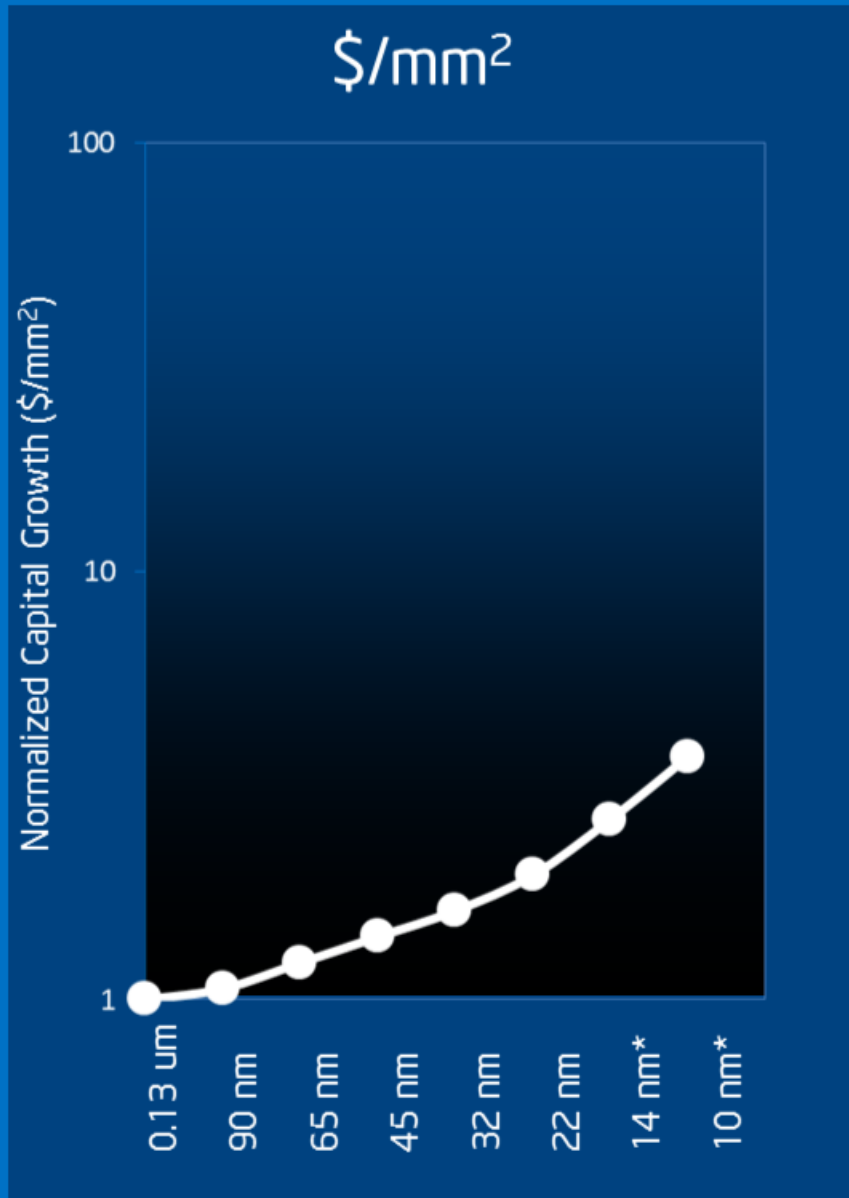
Density Improvements Offset Wafer Cost Trends



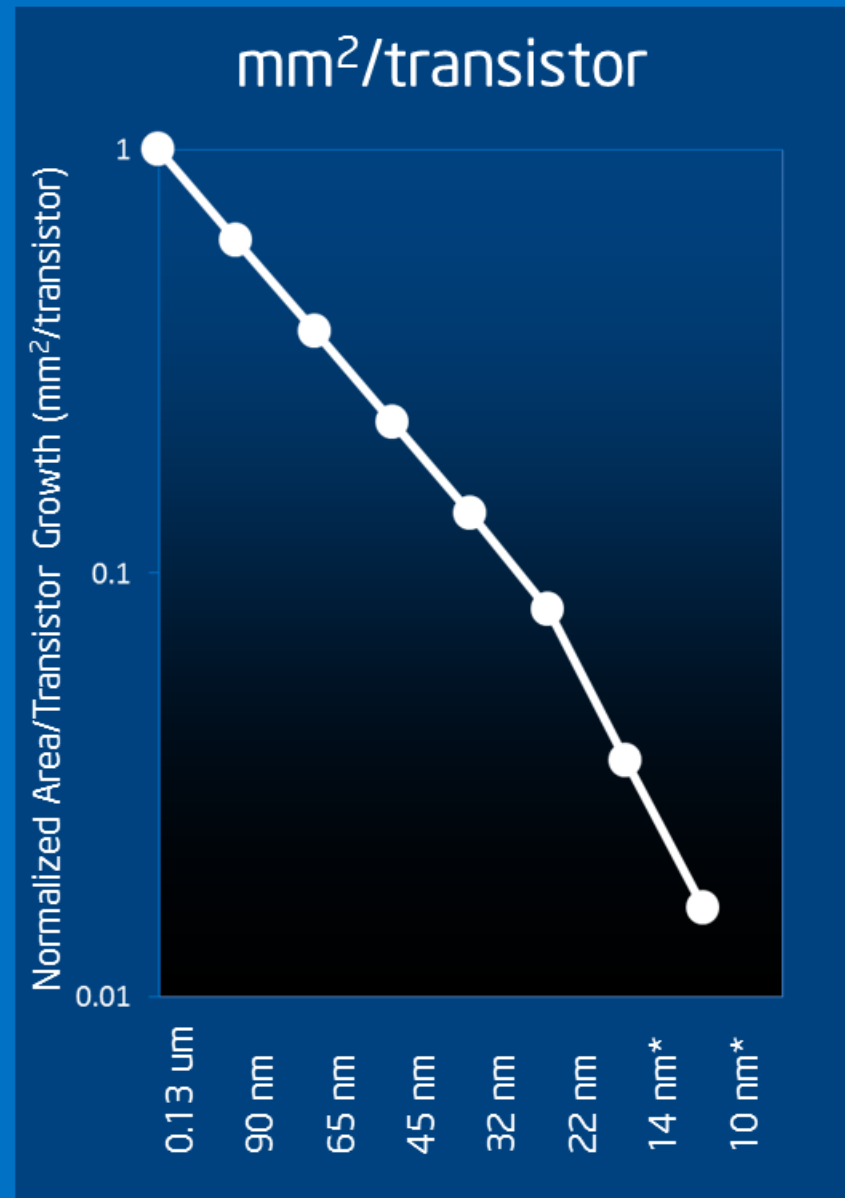
X



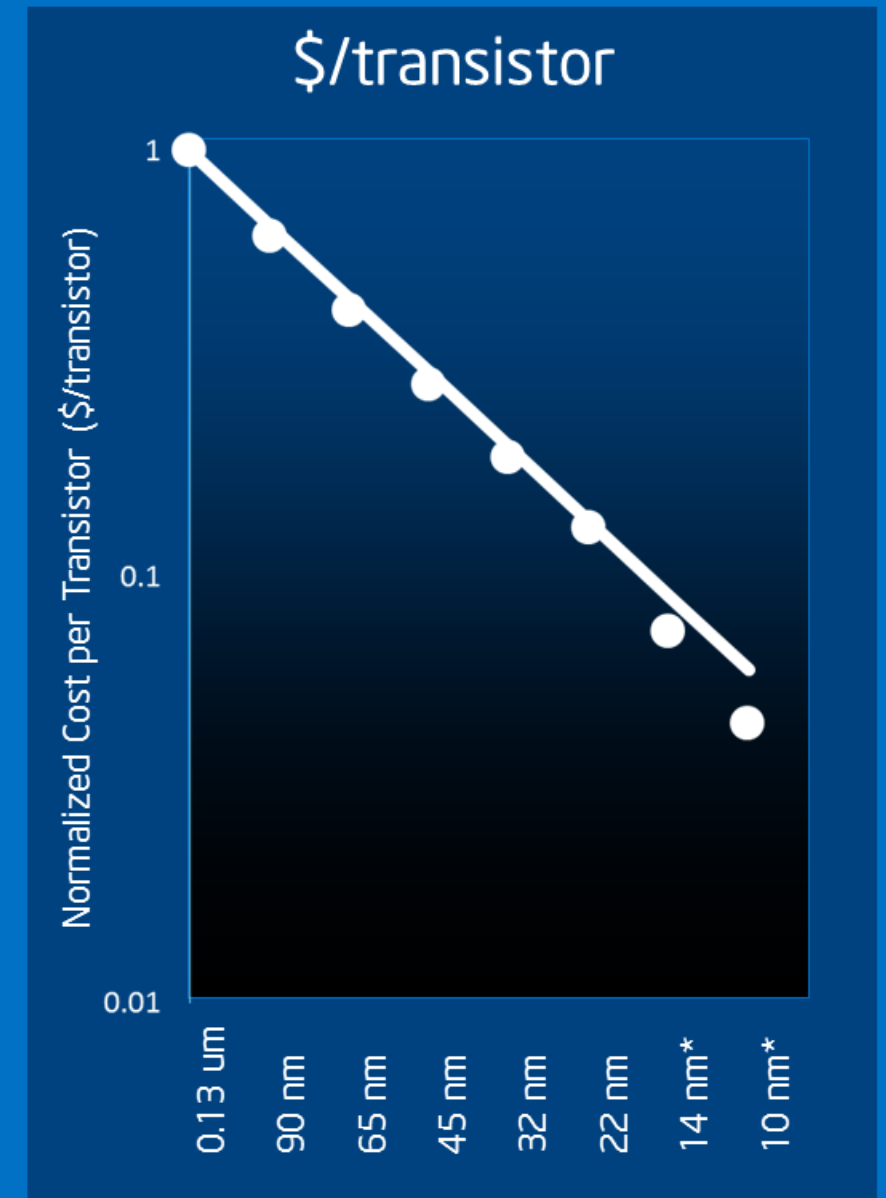
Density Improvements Offset Wafer Cost Trends



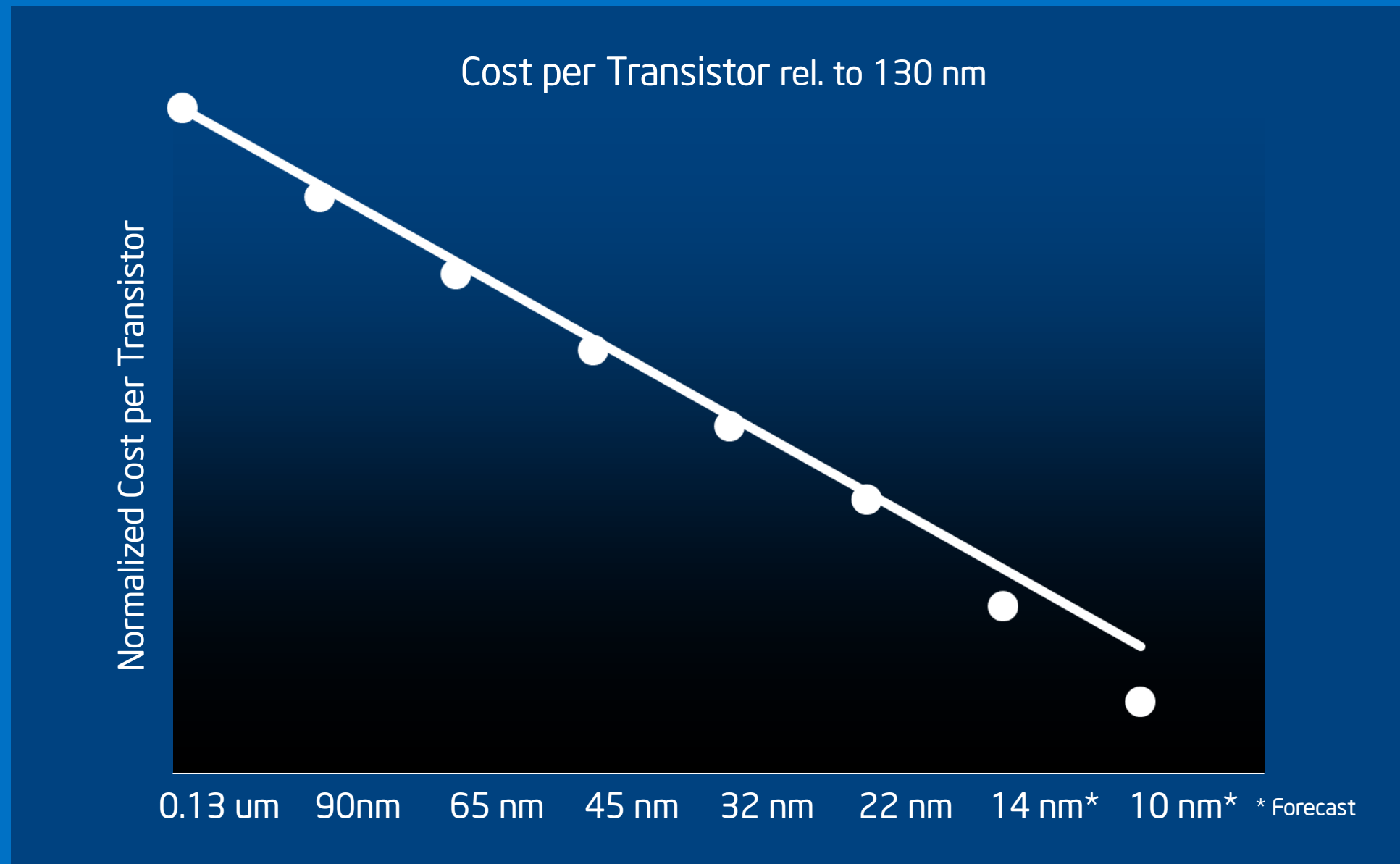
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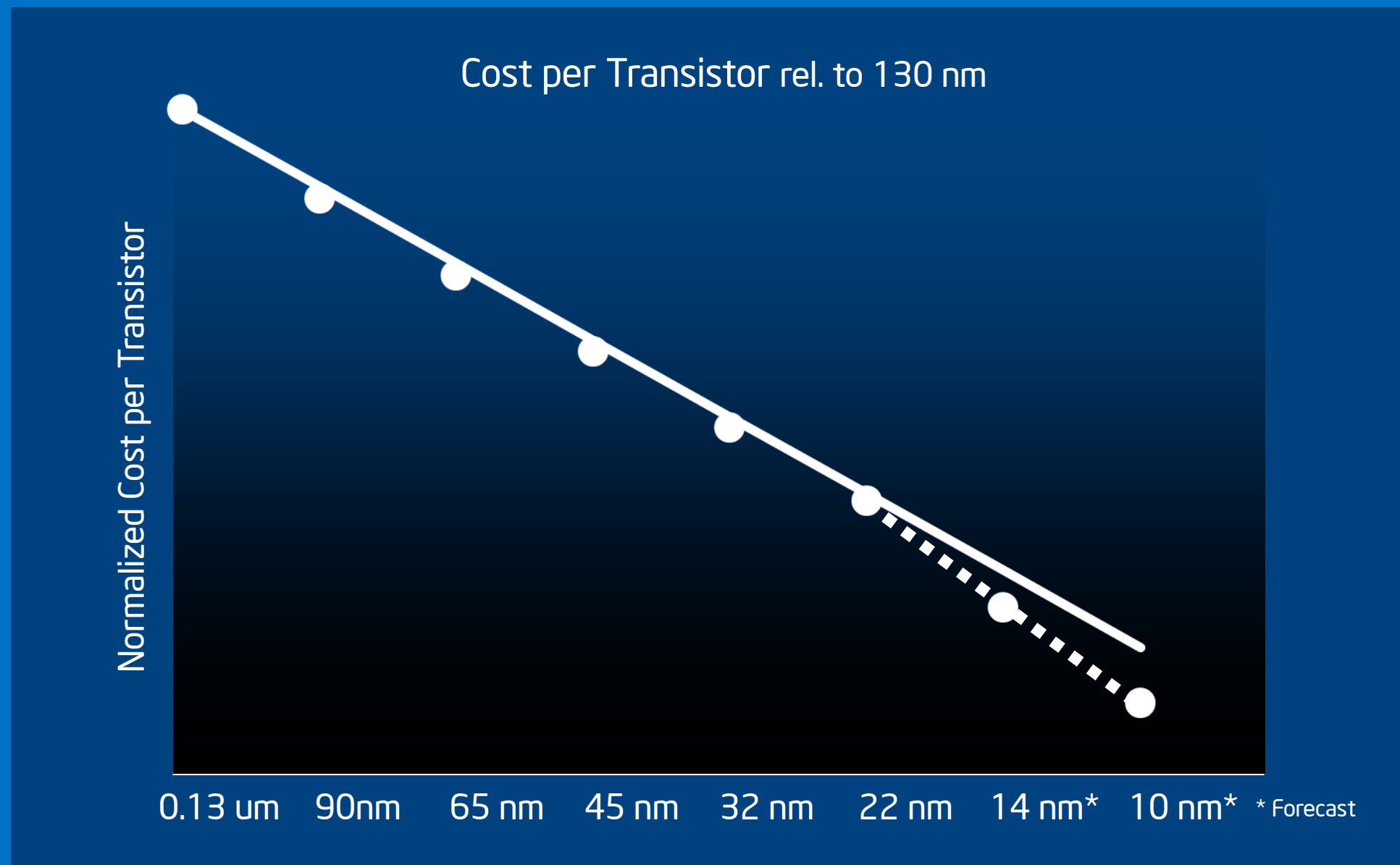
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Density Scaling Continues Cost Improvement



Density Scaling ~~Continues~~ Cost Improvement Accelerates

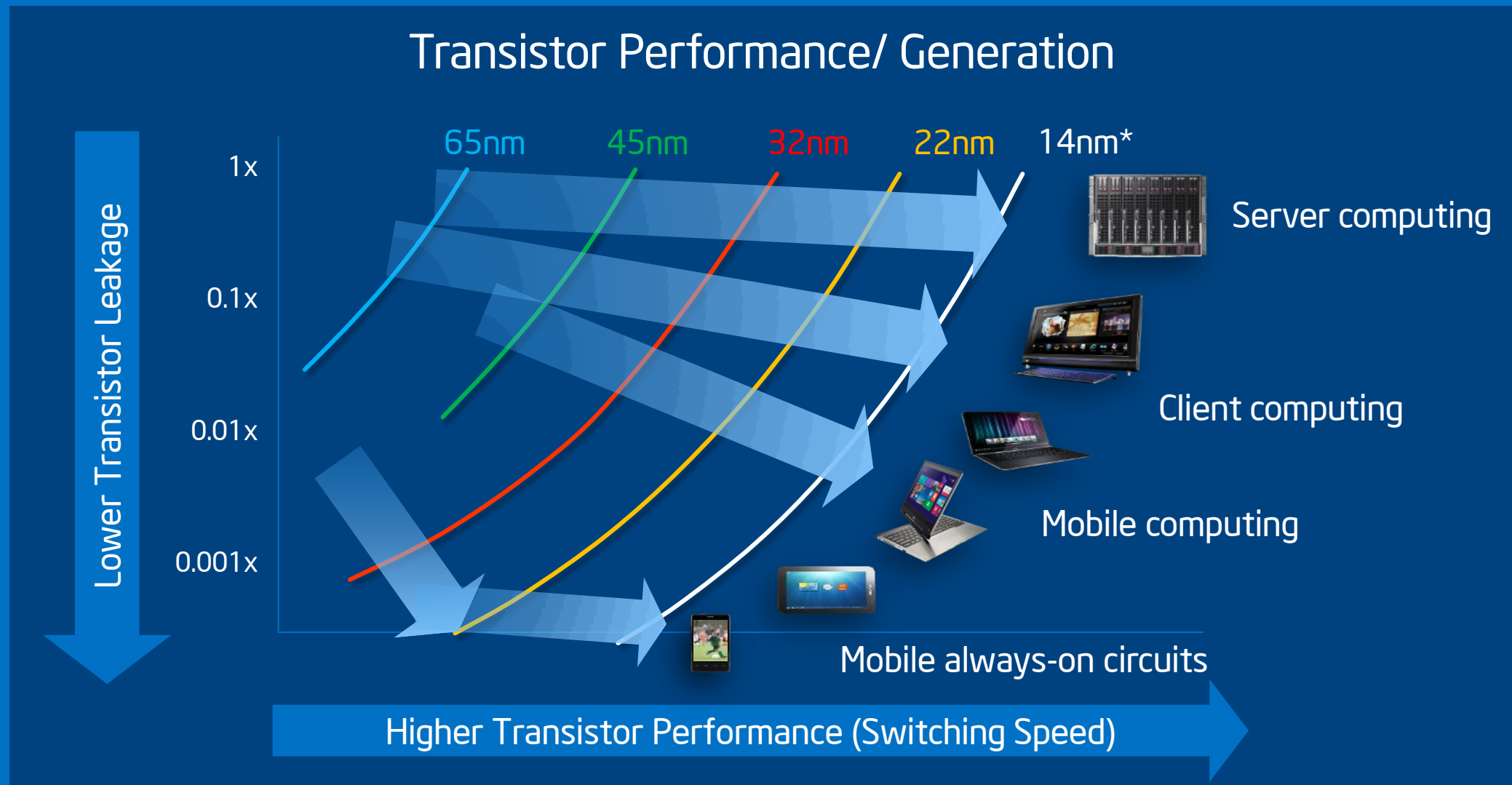


Fundamentals of Moore's Law

Reducing Cost in a Capital Intensive Environment

Applying the Benefits Across the Product Portfolio

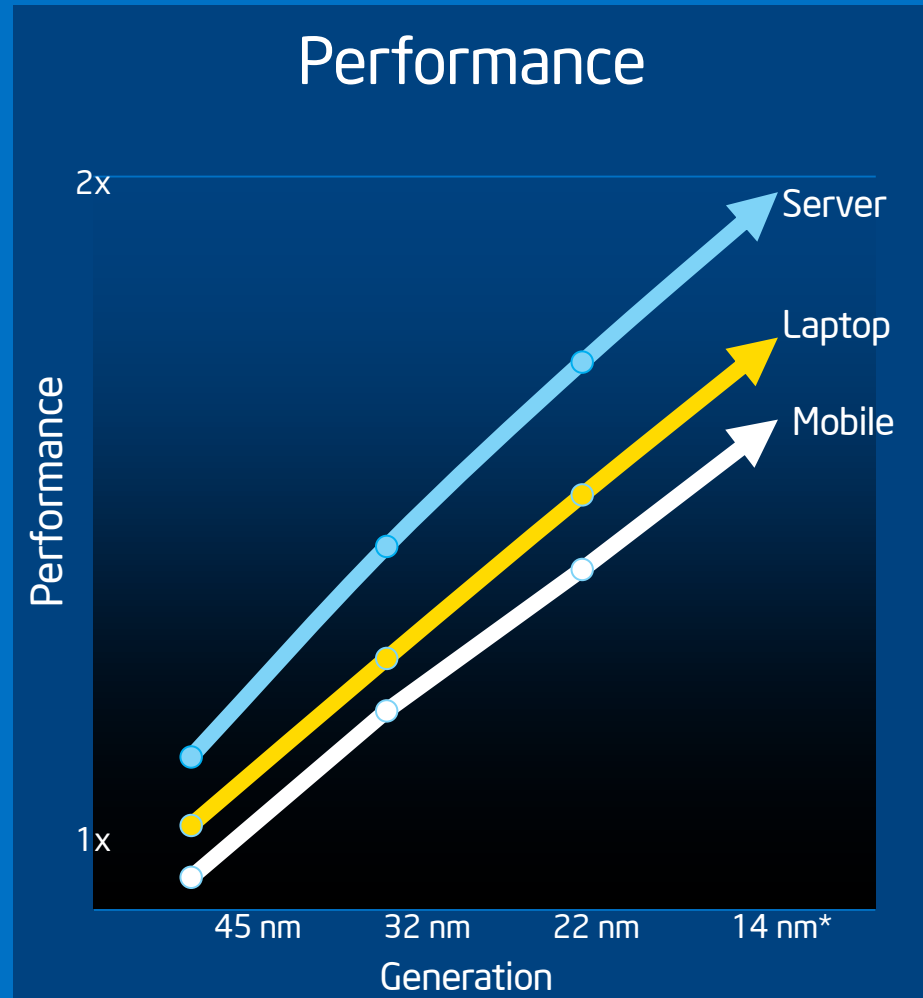
The Value of Better Transistors



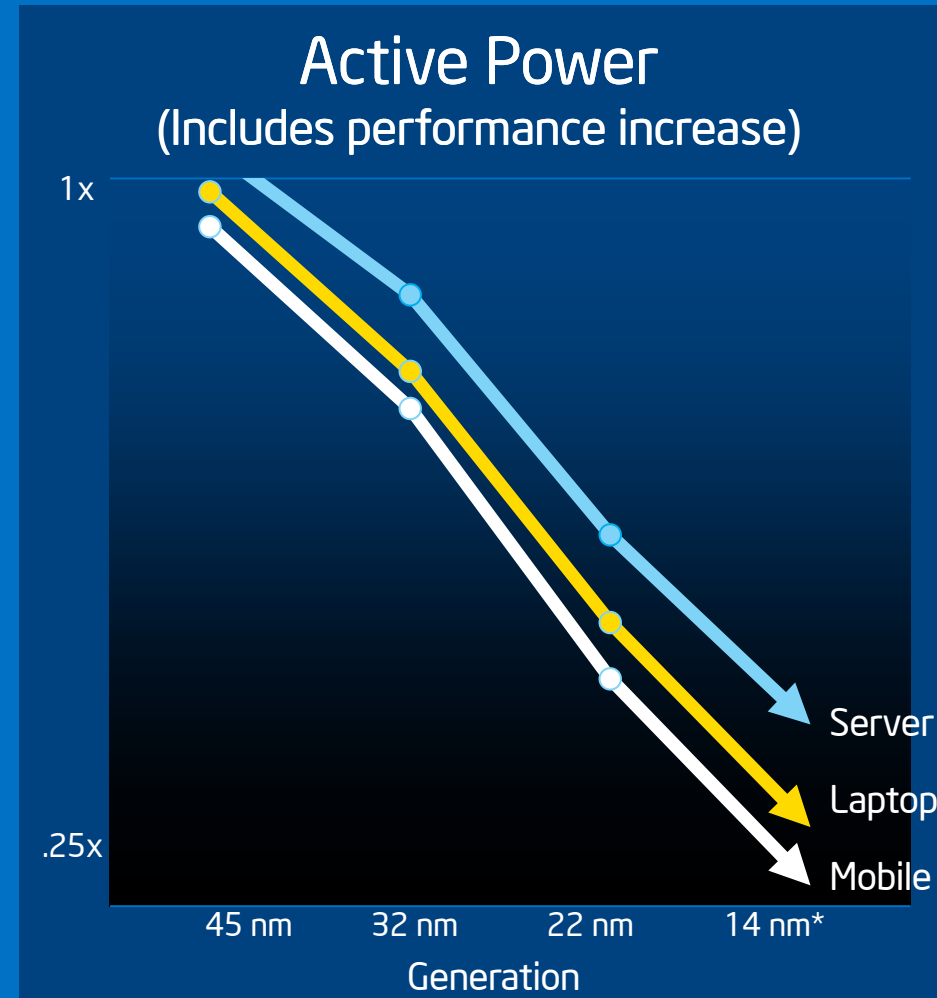
14nm: Continuing the Historical Gains

* Forecast
Source: Intel

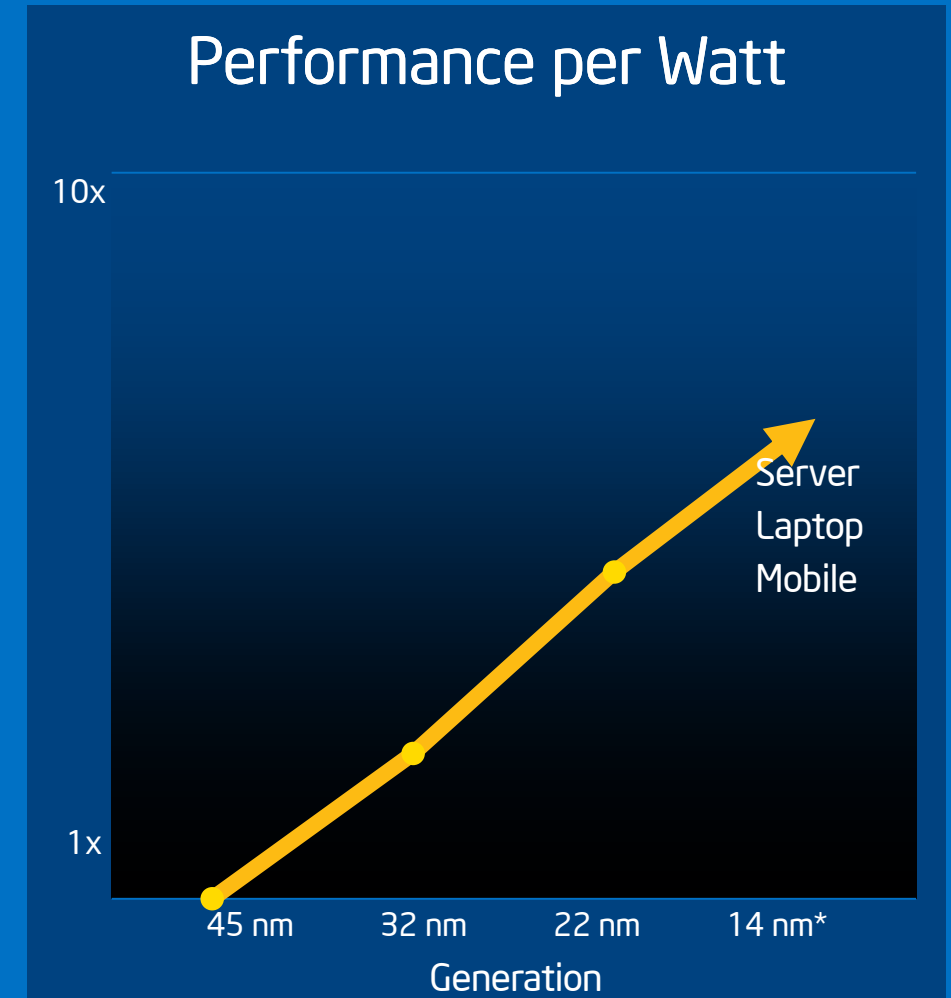
Different Improvement Focus for Different Segments



*Performance Improved
for All Product Families*



*Active Power Reduced
for All Product Families*

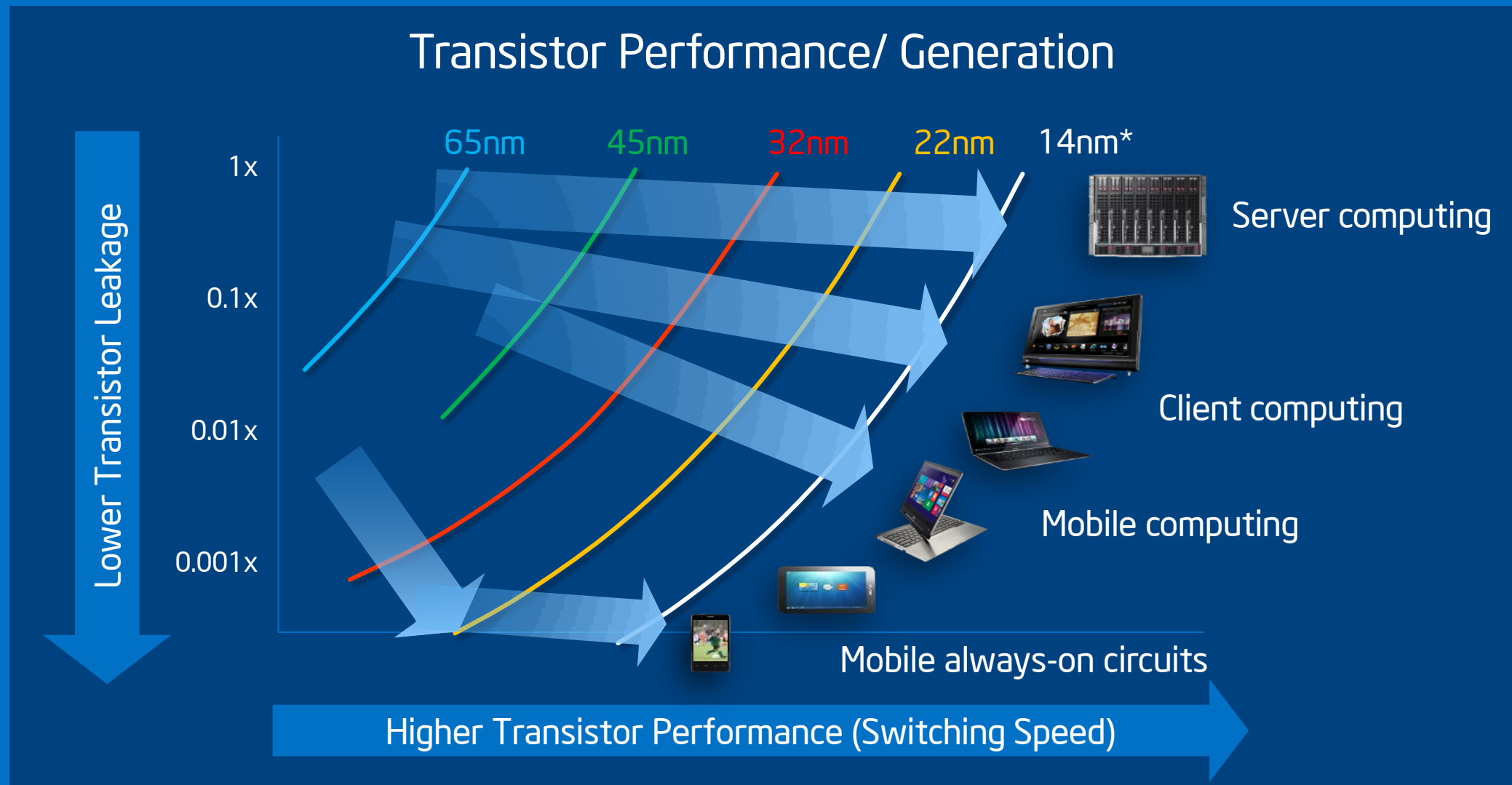


*Performance per Watt Improves
>1.6x per Generation*

Performance per Watt is the Critical enabler for all

* Forecast
Source: Intel

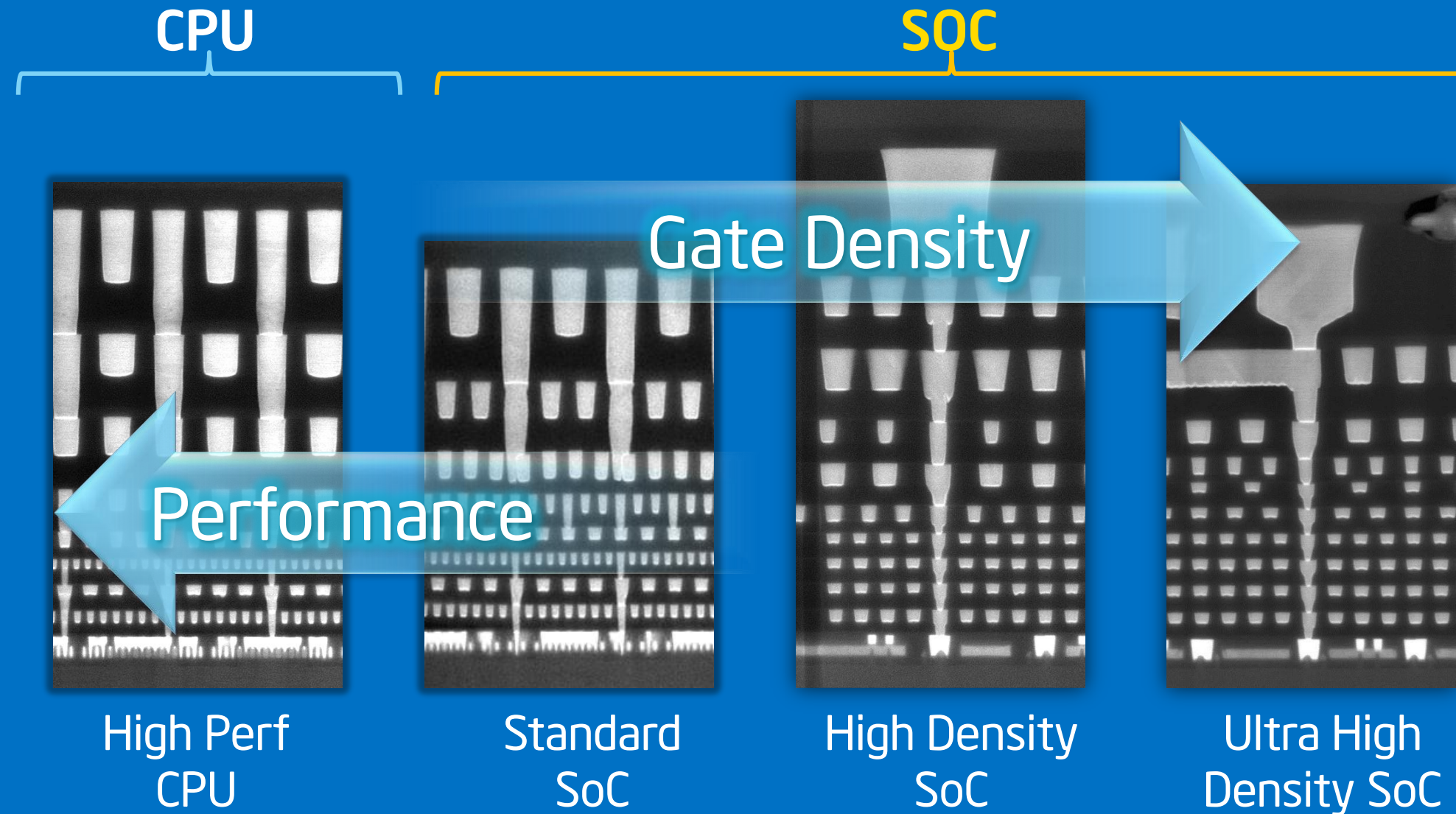
The Value of Better Transistors



The Same Fundamental Improvement Benefits a Wide Range of Products

* Forecast
Source: Intel

Interconnects Options Enable Product Optimization

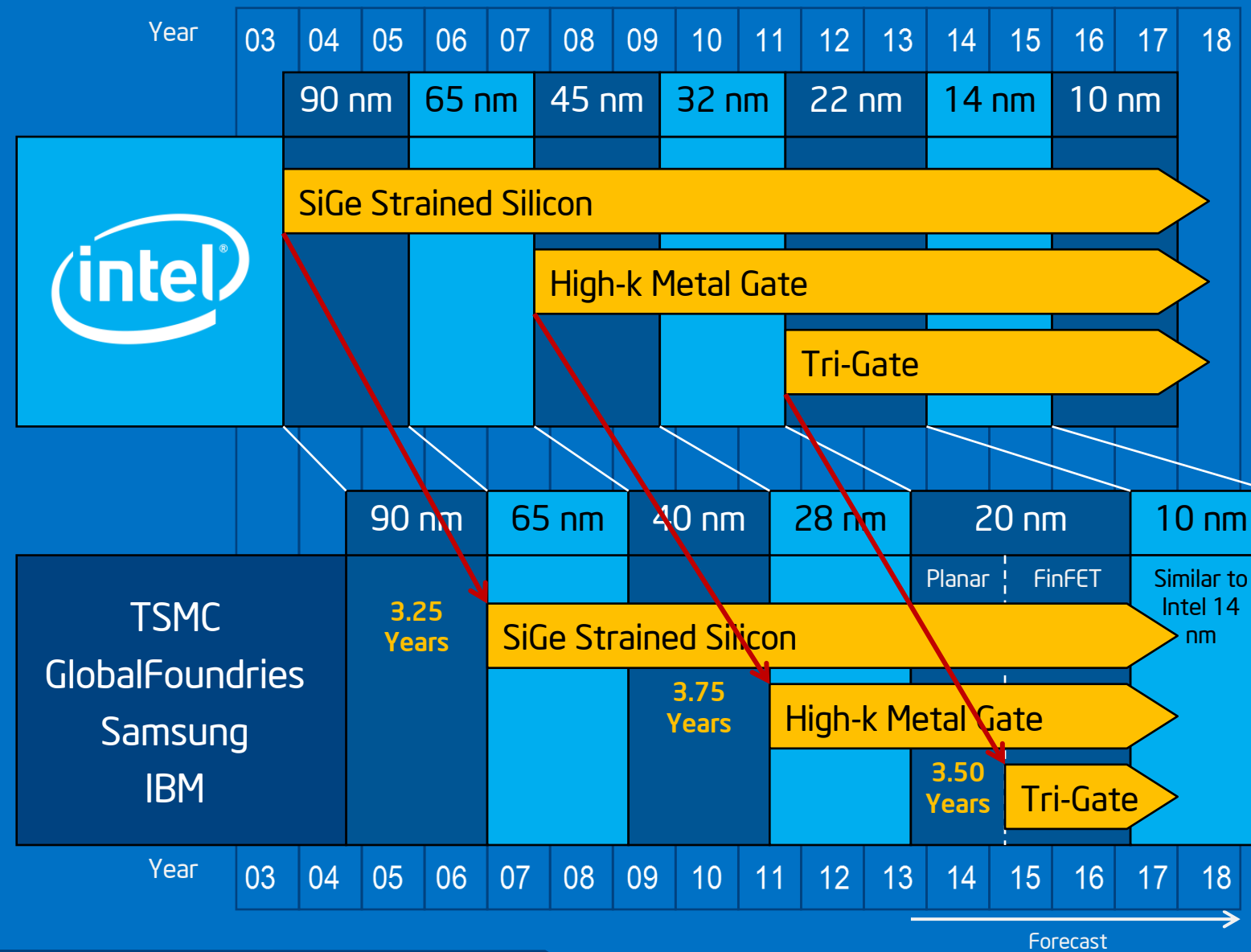


CPU Interconnects Focused on Performance
SoC Interconnects Focused on Density

Expanding the Breadth of Technology Options

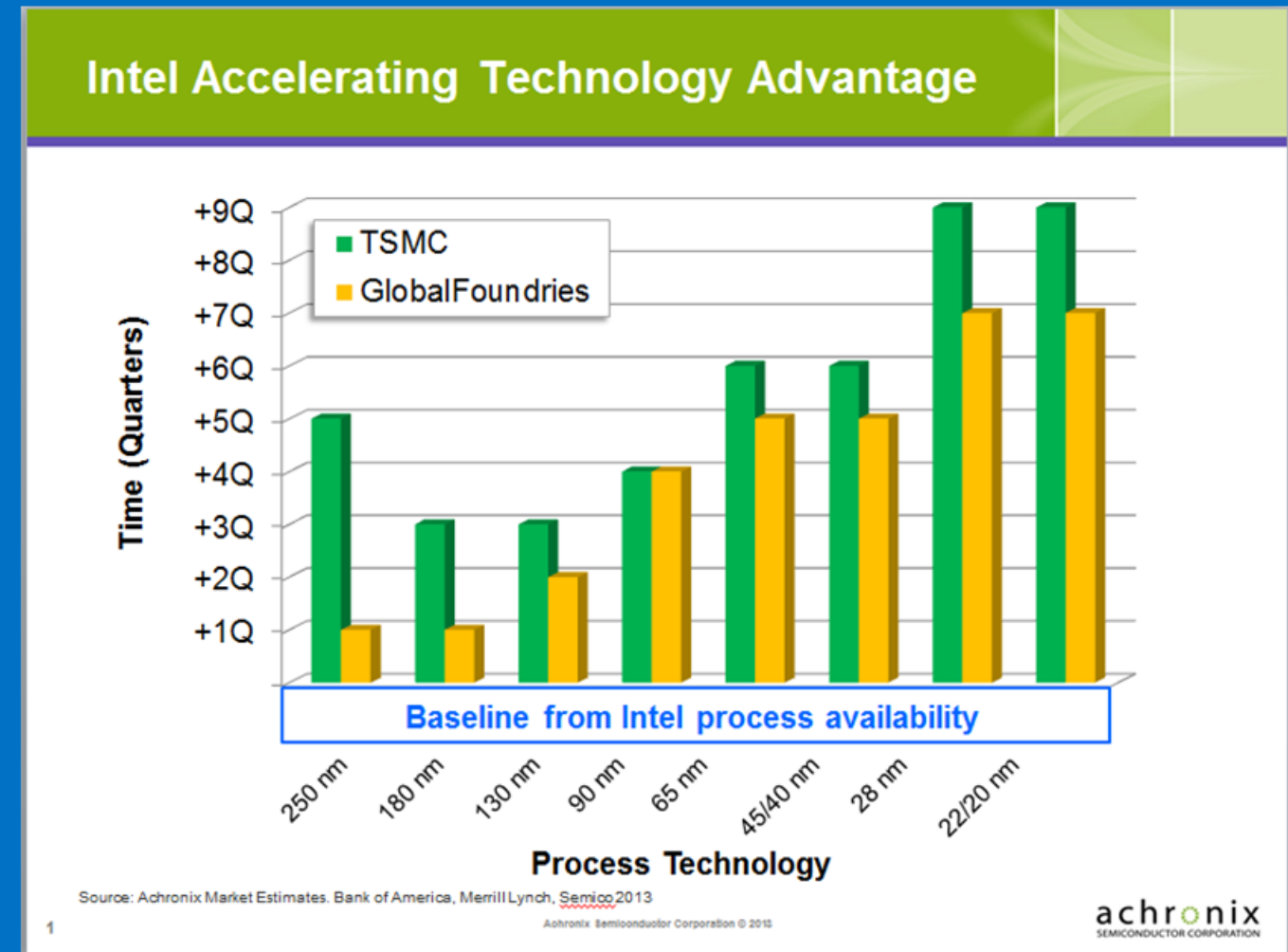
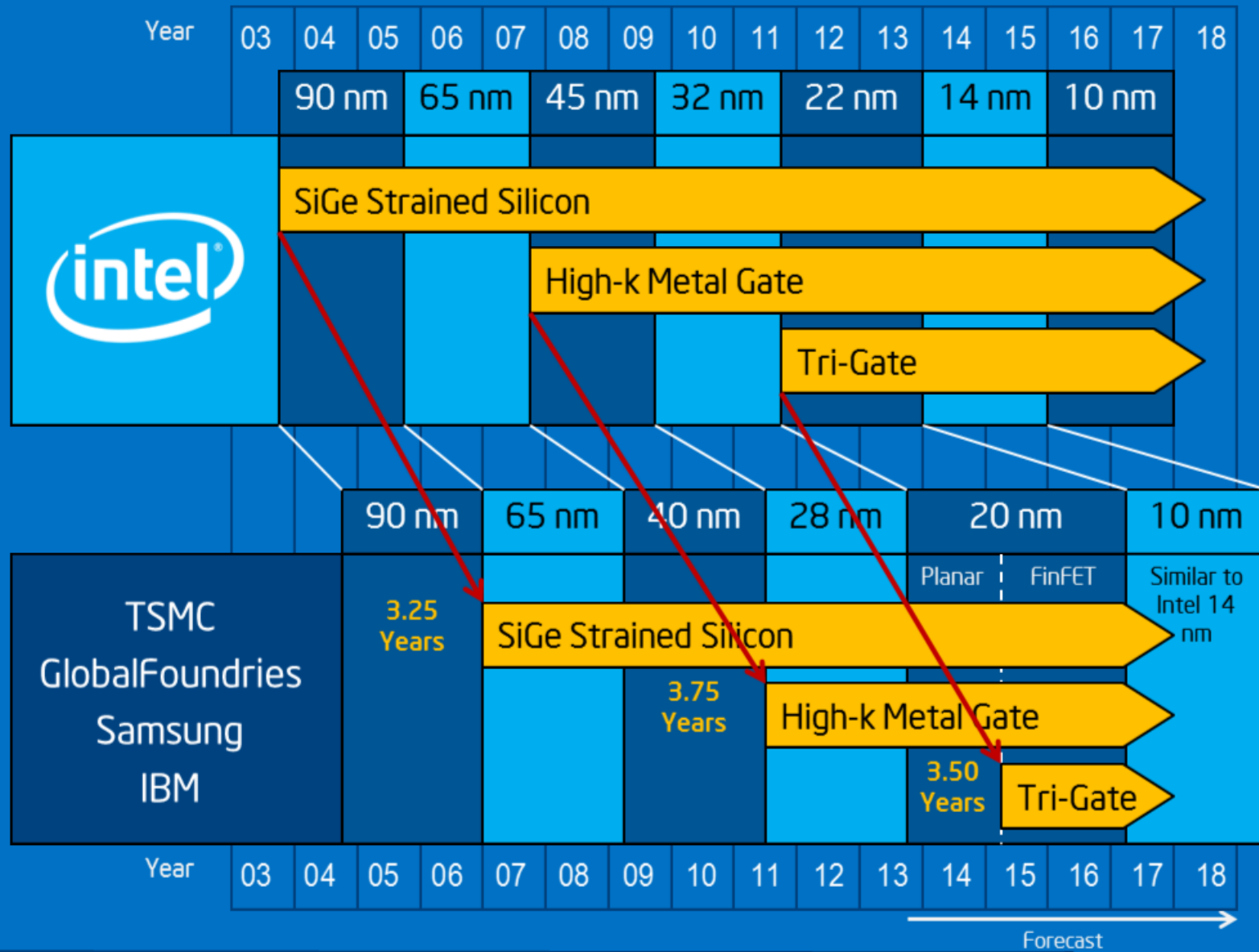
Intel										Intel Custom Foundry			
Features	Options	Client/ Server	Chipsets	Tablets	Embedded DRAM	Wireless Products	Smart Phones	Entry Mobile	FPGA/ ASIC				
Logic Transistor	HP - High Perf.	●							●				
	SP - Std. Perf/Pwr		●	●	●	●	●	●	●				
	LP - Low Power		●			●	●	●					
I/O Transistor	1.2V	●				●	●		●				
	1.8V			●	●	●	●	●	●				
	3.3V		●										
Interconnect	RC Performance	●											
	High Density		●	●			●		●				
	Low Cost					●		●					
	COB				●								
Embedded Memory	e-SRAM - High Performance	●							●				
	e-SRAM - Low Voltage	●	●	●				●					
	e-SRAM - Low Power		●			●	●						
	e-SRAM - Dual Port								●				
	e-PROM/OTP	●	●	●	●	●	●	●	●				
	e-DRAM				●								
Basic Analog/ Passives	Resistor - Linear	●	●	●	●	●	●	●	●				
	Capacitor - MOS, MFC	●	●	●	●	●	●	●	●				
	Capacitor - MIMCAP	●		●			●		●				
	Inductor - Standard	●		●		●		●	●				
Library	High Performance	●							●				
	General Purpose	●	●	●	●		●	●	●				
	High Density		●	●		●	●	●	●				
Adv. Mixed Signals/ RF	Transistor - PA					●							
	Resistor - Precision		●	●		●	●	●	●				
	Capacitor - Linear					●							
	Inductor - High Q					●							
	Deep Nwell/Triple Well					●							
	High Res Substrate					●							

Intel Technology Leadership



Intel Has ~3.5 Year Lead In Introducing Revolutionary Transistor Technologies

Intel Technology Leadership



Source: Achronix, Leading the Industry, Achronix Now Shipping Intel 22nm FPGAs, November 7th, 2013

Intel Has ~3.5 Year Lead In Introducing Revolutionary Transistor Technologies

Summary

Intel Continues to Deliver the Benefits of Moore's Law

True Cost Reduction Remains Possible in a Capital Intensive Environment

The Benefits of Technology Apply Across the Product Portfolio



Risk Factors

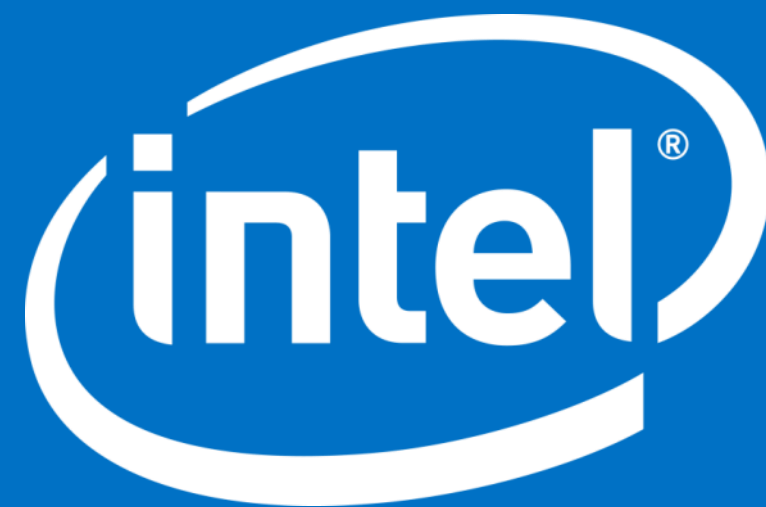
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